

Description

DAMASCENE PROCESS CAPABLE OF AVOIDING VIA RESIST POISONING

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a process for fabricating a metal interconnect, and more particularly, to a damascene process capable of avoiding via resist poisoning.

[0003] 2. Description of the Prior Art

[0004] At present, metal interconnects of the sub-90nm integrated circuit manufacturing process are formed by the damascene process and with a 193nm resist. The damascene process etches a dielectric layer to form a pattern of a metal conductor wire, and then fills the pattern with metal. However, the conventional process needs to dry etch a metal layer and then fill the dielectric layer. Therefore, the damascene process is very important in metal interconnect manufacturing that is unsuitable to dry etch a

metal layer, such as Cu. The damascene process could be sub-classified into a single damascene process and a dual damascene process.

[0005] Please refer to Fig.1 to Fig.3, which show the process schematics according to the single damascene of the prior the art. As shown in Fig.1 to Fig.3, the single damascene of the prior art could be classified into the following three main stages after finishing the conductor plug of the pre-layer (not shown). In the first-stage, as shown in Fig.1, a base layer 10, such as SiN, is deposited. Next, a low-k dielectric layer 12 is deposited over the base layer 10 followed by a SiC layer 14 being deposited over the low-k dielectric layer 12. In the second-stage, as shown in Fig.2, a bottom anti-reflection coating (BARC) layer 16 is formed over the SiC layer 14, a resist layer 18 having a opening 19 to exposure a portion of the BARC layer 16 is formed over the BARC layer 16. In the third-stage, as shown in Fig.3, a single damascene structure 12 is formed in the low-k dielectric layer 12 by etching through the BARC layer 16 and the SiC layer 14 and etching the low-k dielectric layer 12. Then, a metal layer is deposited (not shown). A CMP process removes the metal residues over the low-k dielectric layer 12.

[0006] Please refer to Fig.4 to Fig.10, which show the process schematics according to the dual damascene of the prior art. As shown in Fig.4 to Fig.10, the dual damascene of the prior art could be classified into the following seven main stages after finishing the conductor wire of the pre-layer (not shown). In the first-stage, as shown in Fig.4, a base layer 20, such as SiN, is deposited. A low-k dielectric layer 22 is deposited over the base layer 20. A SiC layer 24 is deposited over the low-k dielectric layer 22. A metal layer 26 is deposited over the SiC layer 24 to be a hard mask. A first BARC layer 28 is deposited over the metal layer 26. A dielectric layer (not shown) could be set between the metal layer 26 and the first BARC layer 28. A first resist layer 32 is formed having a trench opening 30, called a trench photo. In the second-stage, as shown in Fig.5, a trench structure 34 is formed by etching through first BARC layer 28, the metal layer 26, and a portion of the SiC layer 24 through the trench opening 30. In the third-stage, as shown in Fig.6, the first resist layer 32 and the first BARC layer 28 are removed.

[0007] In the fourth-stage, as shown in Fig.7, a second BARC layer 36 is deposited over the SiC layer 24 and the metal layer 26, the second BARC layer 36 filling the trench

structure 34. Next, a second resist layer 40 is formed having a via opening 38, called as via photo. In the fifth-stage, as shown in Fig.8, a via structure 42 is formed by etching through the second BARC layer 36, the SiC layer 24, and a portion of the low-k dielectric layer 22 through the via opening 38.

[0008] In the sixth-stage, as shown in Fig.9, the second resist layer 40 and the second BARC layer 36 are removed. In the seventh-stage, as shown in Fig.10, a dual damascene structure having the trench and the via structure is formed in the low-k dielectric layer 22 by using the metal layer 26 and the SiC layer 24 as masks. Then, a metal layer (not shown) is deposited over the low-k dielectric layer 22. A CMP process removes the metal residues on the low-k dielectric layer 22.

[0009] However, a serious problem in the damascene process of the prior art is a via resist poisoning phenomenon. The above low-k dielectric layers 12, 22 of the damascene process of the prior art contain unpolymerized precursors. The unpolymerized precursors diffuse out from the low-k dielectric layers 12, 22, and the thickness of the SiC layers 14, 24 is insufficient to prevent unpolymerized precursors diffused out from the low-k dielectric layers 12, 22 from

contacting an overlying resist. The unpolymerized precursors react with the subsequent resist layers 18, 22 to form a resist scum defect or via missing defect.

SUMMARY OF INVENTION

[0010] It is therefore a primary object of the claimed invention to provide a damascene process capable of avoiding via resist poisoning.

[0011] According to the claimed invention, a semiconductor substrate with a low- k dielectric layer ($k \leq 2.9$) thereon and a SiC layer over the low- k dielectric layer is provided. A blocking layer is formed on the SiC layer, where the blocking layer is used to prevent unpolymerized precursors diffused out from the low- k dielectric layer from contacting an overlying resist. A BARC layer is formed on the blocking layer. A resist layer having an opening to expose a portion of the BARC layer is formed on the BARC layer. A damascene structure is formed in the low- k dielectric layer by etching through the BARC layer, the blocking layer, the SiC layer, and a portion of the low- k dielectric layer through the opening.

[0012] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the pre-

ferred embodiment, which is illustrated in the multiple figures and drawings.

BRIEF DESCRIPTION OF DRAWINGS

[0013] Fig.1 to Fig.3 show the process schematics according to the single damascene of the prior art.

[0014] Fig.4 to Fig.10 show the process schematics according to the dual damascene of the prior art.

[0015] Fig.11 and Fig.12 show the process schematics according to the first embodiment of the present invention.

[0016] Fig.13 to Fig.16 show the process schematics according to the second embodiment of the present invention.

DETAILED DESCRIPTION

[0017] Please refer to Fig.11 and Fig.12, which show the process schematics according to the first embodiment of the present invention. The first embodiment of the present invention includes three main stages as previously described in the single damascene process of the prior art section of this application. Since the first-stage of the first embodiment of the present invention is substantially the same as the prior art, further elaboration is omitted here for the sake of simplicity. The discussion of the first embodiment will now begin on the second-stage. In the sec-

ond-stage, as shown in Fig. 11, a blocking layer 15 on the surface of the SiC layer 14 is formed by Ar plasma hitting the SiC layer 14. The blocking layer 15 is used to prevent unpolymerized precursors diffused out from the low-dielectric layer ($k \leq 2.9$) 12 from contacting a subsequent overlying resist (not shown).

[0018] The above low-k dielectric layer 12 comprises a carbon-doped oxide (CDO) substance. The thickness of the SiC layer 14 is less than 700 angstroms. The Ar plasma comprises a flurane substance. The flurane substance could be CF_4 . However, the present invention is not limited in this way.

[0019] Next, a BARC layer 16 is formed on the blocking layer 15. A resist layer 18 having a via opening 19 to expose a portion of the BARC layer 16 is formed on the BARC layer 16.

[0020] In the third-stage, as shown in Fig. 12, a single damascene structure is formed in the low-k dielectric layer 12 by etching through the BARC layer 16, the blocking layer 15, the SiC layer 14, and a portion of the low-k dielectric layer 12. Then, a metal layer (not shown) is deposited over the low-k dielectric layer 12. A CMP process removes the metal residues on the low-k dielectric layer 12.

[0021] Please refer to Fig.13 to Fig.16, which show the process

schematics according to the second embodiment of the present invention. The second embodiment of the present invention includes the seven main stages shown in Fig.4 to Fig.10 as previously described in the dual damascene process of the prior art section of this application. Since the second embodiment of the present invention from the first-stage to the third-stage is substantially the same as the prior art, further elaboration here is omitted for the sake of simplicity. The discussion of the first embodiment will now begin on the fourth-stage. In the fourth-stage, as shown in Fig. 13, a blocking layer 35 on the surface of the trench structure 34 of the SiC layer 24 is formed by Ar plasma hitting the SiC layer 24, where the blocking layer 35 is used to prevent unpolymerized precursors diffused out from the low-k dielectric layer 22 from contacting an overlying resist.

[0022] The above low-k dielectric layer 22 comprises a CDO substance. The thickness of the SiC layer 24 is less than 700 angstroms. The Ar plasma comprises a flurane substance. The flurane substance could be CF_4 . However, the present invention is not limited in this way.

[0023] A second BARC layer 36 is formed on the blocking layer 35 and the metal layer 26, the second BARC layer 36 fill-

ing the trench structure 34. A second resist layer 40 having a via opening, called a via photo, to expose a portion of the second BARC layer 36 is formed on the second BARC layer 36. In the fifth-stage, as shown in Fig.14, the via opening 38 is utilized to etch through the second BARC layer 36, the blocking layer 35, the SiC layer 24, and a portion of the low-k dielectric layer 22 to form a via structure 42.

[0024] In the sixth-stage, as shown in Fig.15, the second resist layer 40 and the second BARC layer 36 are removed. In the seventh-stage, as shown in Fig.16, a dual damascene structure having the trench and the via structure is formed in the low-k dielectric layer 22 by using the metal layer 26 and the SiC layer 24 as masks. A metal layer is deposited (not shown). A CMP process removes the metal residues on the low-k dielectric layer 22.

[0025] Those skilled in the art will readily observe that numerous modification and alterations of the process may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.